

VLSI Design

Lecture 3: Transistor Characteristics

Shaahin Hessabi

Department of Computer Engineering

Sharif University of Technology

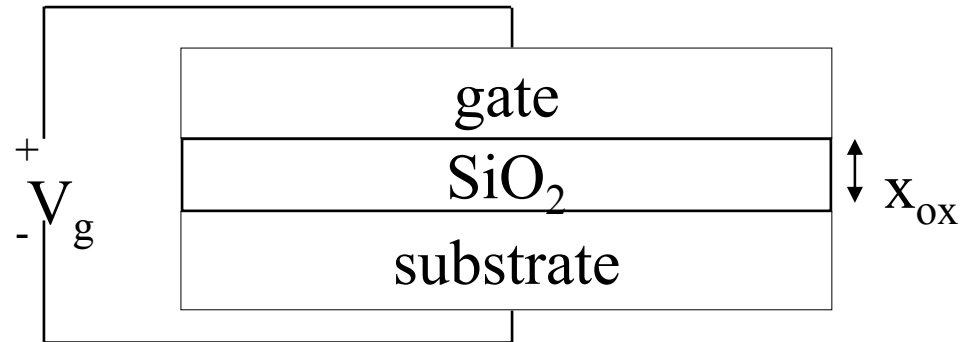
Adapted, with modifications, from lecture notes prepared by the
author (from Prentice Hall PTR)

Topics

- Derivation of transistor characteristics.
- Simulation

MOSFET gate as capacitor

- Basic structure of gate is parallel-plate capacitor



- Formula for parallel plate capacitance:

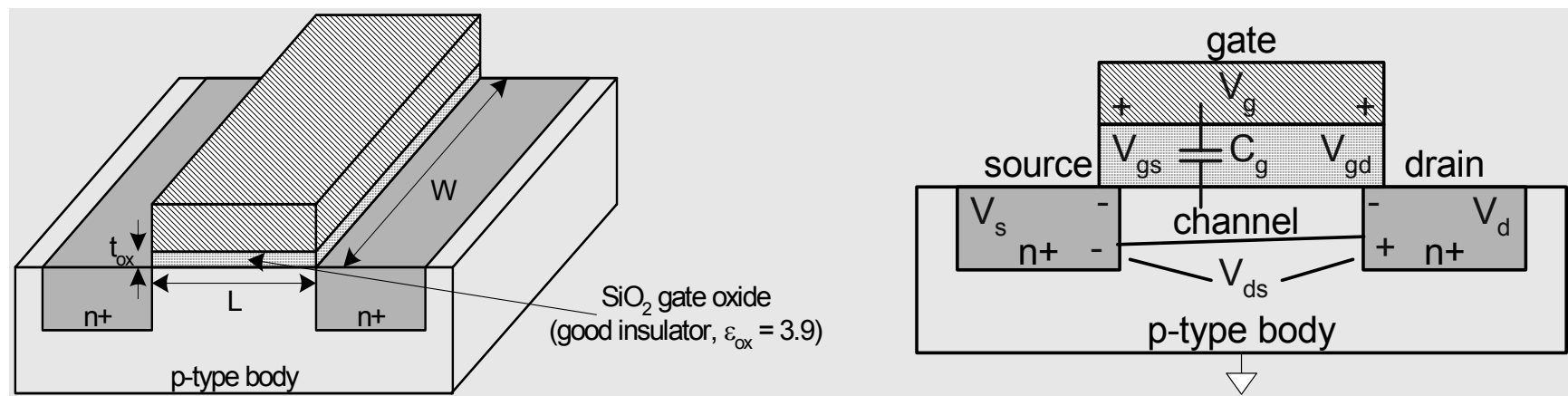
$$C_{ox} = \epsilon_{ox} / x_{ox}$$

❖ Permittivity of silicon: $\epsilon_{ox} = 3.46 \times 10^{-13} \text{ F/cm}$

- Gate capacitance helps determine charge in channel which forms inversion region.

Parallel plate capacitance

- Mobile electrons move if voltage applied between S and D
- $Q_{\text{channel}} = CV$
- $C = C_g = C_{\text{ox}} WL = \epsilon_{\text{ox}} WL / x_{\text{ox}}$
- $V = V_{\text{gc}} - V_t = (V_{\text{gs}} - V_{\text{ds}}/2) - V_t$



Carrier Velocity

- Charge is carried by e-
- Carrier velocity v proportional to lateral E-field between source and drain
- $v = \mu E$ μ called mobility
- $E = V_{ds}/L$
- Time for carrier to cross channel: $t = L / v$

nMOS Linear I - V

■ Now we know

- ❖ How much charge Q_{channel} is in the channel
- ❖ How much time t each carrier takes to cross

$$\begin{aligned} I_{ds} &= \frac{Q_{\text{channel}}}{t} \\ &= \mu C_{\text{ox}} \frac{W}{L} \left(V_{gs} - V_t - \frac{V_{ds}}{2} \right) V_{ds} \\ &= \beta \left(V_{gs} - V_t - \frac{V_{ds}}{2} \right) V_{ds} \end{aligned} \quad \beta = \mu C_{\text{ox}} \frac{W}{L}$$

Current $\propto V_{gs} - V_t$ since $V_{gs} - V_t$ sets the number of carriers in the channel

Current $\propto C_{\text{ox}} \propto 1/x_{\text{ox}}$

Current $\propto W/L$ -- Resistance $\propto L/W$

nMOS Saturation I-V

- If $V_{gd} < V_t$, channel pinches off near drain
 - ❖ When $V_{ds} > V_{dsat} = V_{gs} - V_t$
- Now drain voltage no longer increases current

$$\begin{aligned} I_{ds} &= \beta \left(V_{gs} - V_t - \frac{V_{dsat}}{2} \right) V_{dsat} \\ &= \frac{\beta}{2} (V_{gs} - V_t)^2 \end{aligned}$$

nMOS I-V Summary

- *Shockley* 1st order transistor models

$$I_{ds} = \begin{cases} 0 & V_{gs} < V_t & \text{cutoff} \\ \beta \left(V_{gs} - V_t - \frac{V_{ds}}{2} \right) V_{ds} & V_{ds} < V_{dsat} & \text{linear} \\ \frac{\beta}{2} (V_{gs} - V_t)^2 & V_{ds} > V_{dsat} & \text{saturation} \end{cases}$$

Threshold voltage

Components of threshold voltage V_t :

- V_{fb} = flatband voltage; depends on difference in work function between gate and substrate and on fixed surface charge.
- ϕ_s = surface potential (about $2\phi_f$).
- Voltage on parallel plate capacitor.
- Additional ion implantation.

Body effect

- Reorganize threshold voltage equation:

$$V_t = V_{t0} + \Delta V_t$$

- Threshold voltage is a function of source/substrate voltage V_{sb} .
- Body effect γ is the coefficient for the V_{sb} dependence factor.

- ❖ $\gamma_n = \text{sqrt}(2q\epsilon_{Si}N_A)/C_{ox}$

- ❖ $V_t = V_{t0} + \gamma_n(\text{sqrt}(\phi_S + V_{sb}) - \text{sqrt}(\phi_S))$

Example: threshold voltage of a transistor

- $V_{t0} = V_{fb} + \phi_s + Q_b/C_{ox} + V_{II}$
 $= -0.91 \text{ V} + 0.58 \text{ V} + (1.4\text{E-}8/1.73\text{E-}7) + 0.92 \text{ V}$
 $= 0.68 \text{ V}$
- Body effect $\gamma_n = \text{sqrt}(2q\epsilon_{Si}N_A/C_{ox}) = 0.1$
- $\Delta V_t = \gamma_n[\text{sqrt}(\phi_s + V_{sb}) - \text{sqrt}(\phi_s)]$
 $= 0.16 \text{ V (for } V_{sb} = 5\text{V)}$
 - ❖ Body effect makes 24% difference in threshold voltage

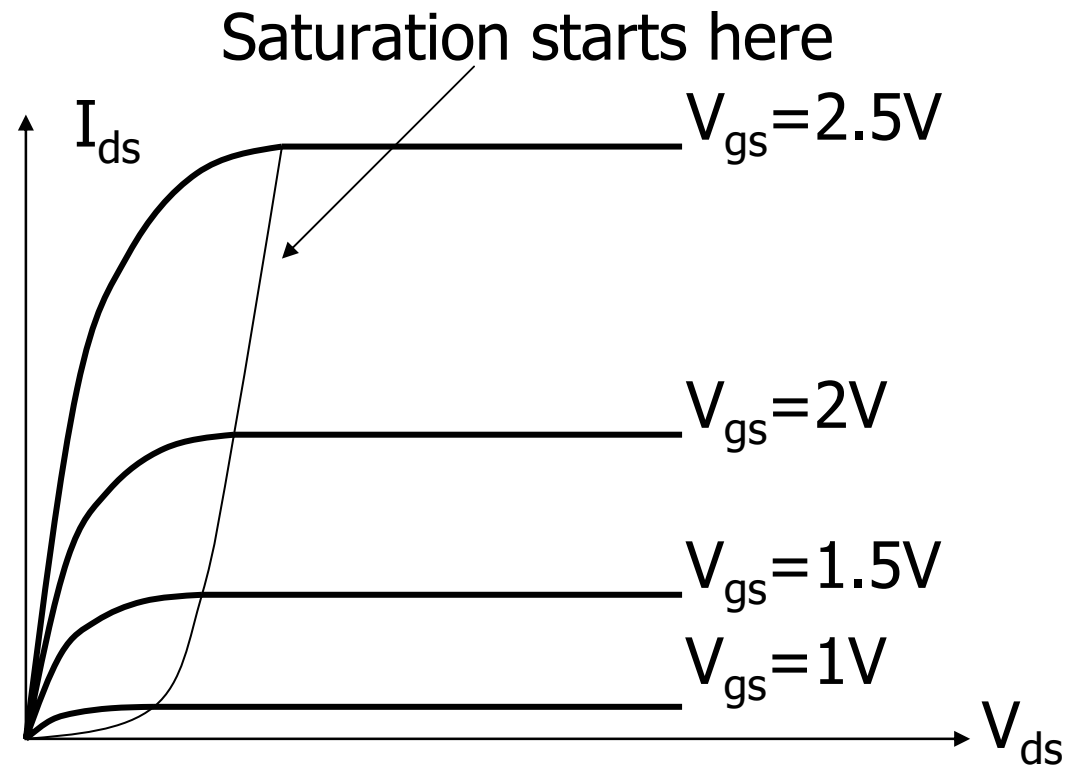
More device parameters

- Process transconductance $k' = \mu C_{ox}$.
- Device transconductance $\beta = k'W/L$.

Channel length modulation

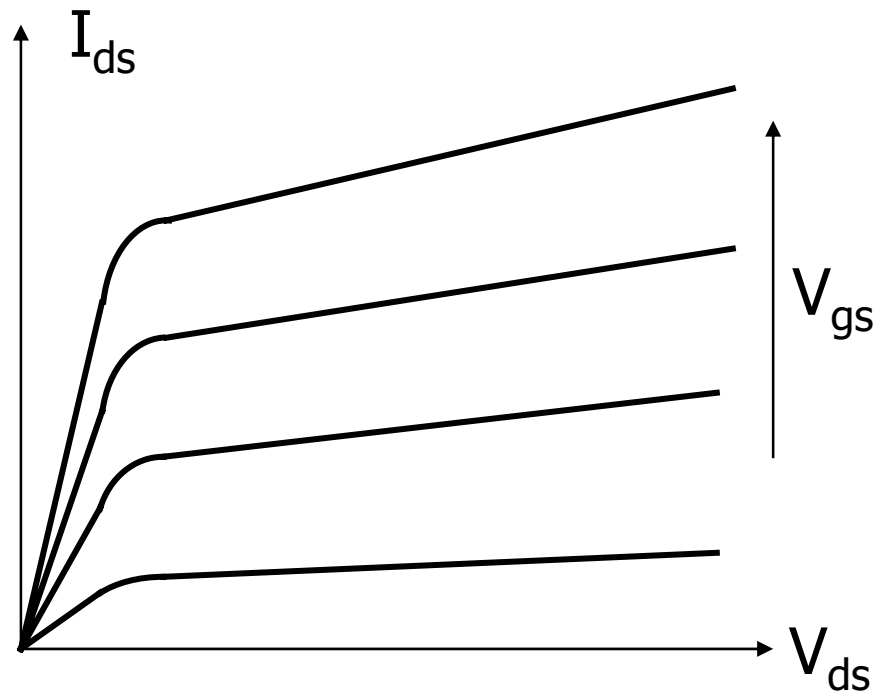
- λ describes small dependence of drain current on V_{ds} in saturation.
- Factor is measured empirically.
- New drain current equation:
 - ❖ $I_d = 0.5k' (W/L)(V_{gs} - V_t)^2(1 + \lambda V_{ds})$
- Equation has a discontinuity between linear and saturation regions---small enough to be ignored.

Ideal Quadratic NMOS I-V Curve



Real NMOS I-V Curve

- Transistor, when conducting, may be modeled as voltage-controlled resistor



Example

- We will be using a 0.6 μm process

- ❖ From AMI Semiconductor

- ❖ $x_{\text{ox}} = 100 \text{ \AA}$

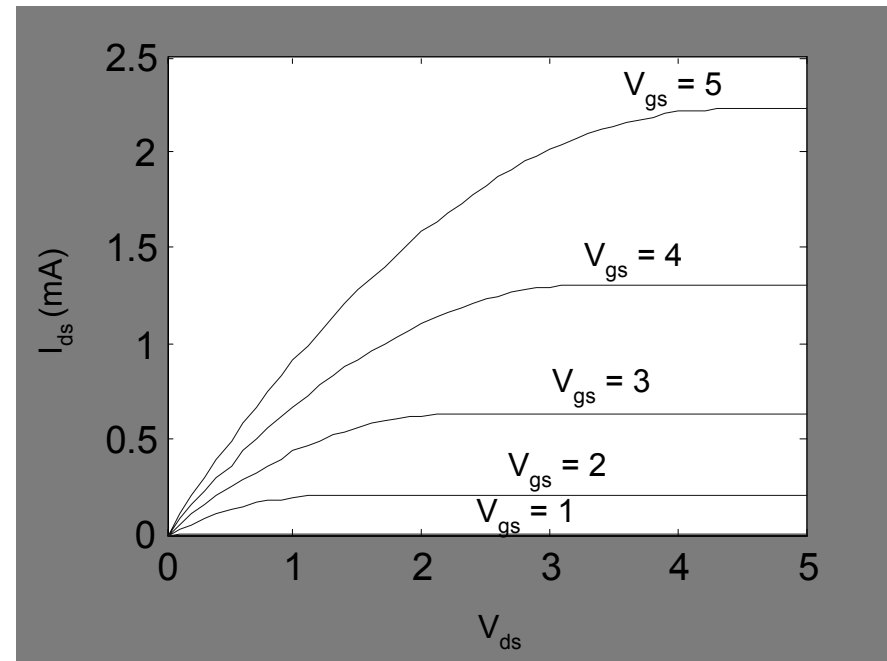
- ❖ $\mu = 350 \text{ cm}^2/\text{V}^*\text{s}$

- ❖ $V_t = 0.7 \text{ V}$

- Plot I_{ds} vs. V_{ds}

- ❖ $V_{\text{gs}} = 0, 1, 2, 3, 4, 5$

- ❖ Use $W/L = 4/2 \lambda$

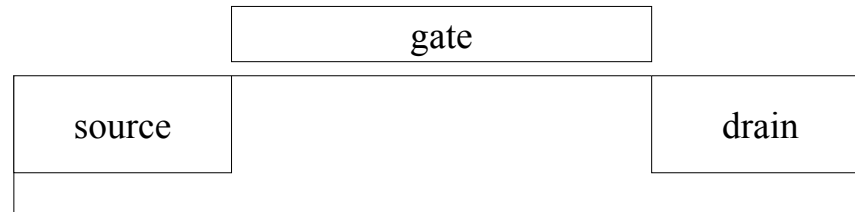


$$\beta = \mu C_{\text{ox}} \frac{W}{L} = (350) \left(\frac{3.9 \cdot 8.85 \cdot 10^{-14}}{100 \cdot 10^{-8}} \right) \left(\frac{W}{L} \right) = 120 \frac{W}{L} \mu\text{A}/\text{V}^2$$

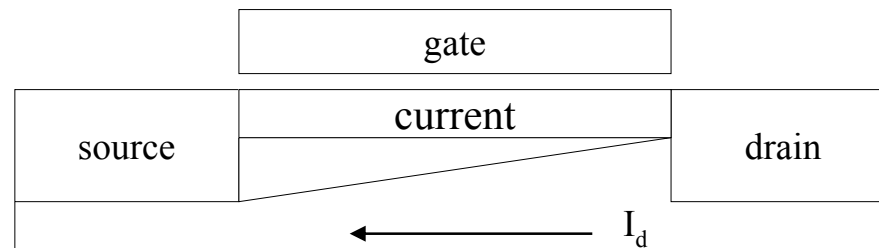
pMOS I - V

- All dopings and voltages are inverted for pMOS
- Mobility μ_p is determined by holes
 - ❖ Typically 2-3 times lower than that of electrons μ_n
 - ❖ $120 \text{ cm}^2/\text{V}\cdot\text{s}$ in AMI $0.6 \mu\text{m}$ process
- Thus pMOS must be wider to provide same current
 - ❖ Assume $\mu_n / \mu_p = 2$ (depends on technology)

Gate voltage and the channel

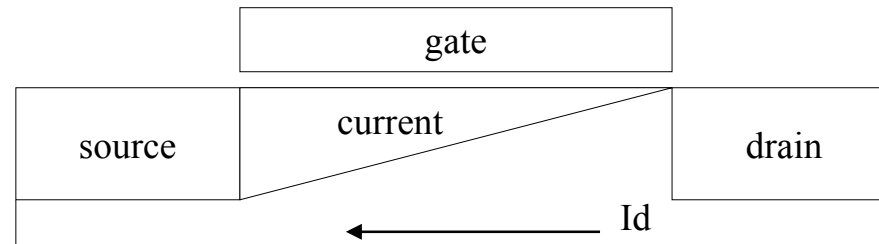


$$V_{gs} < V_t$$



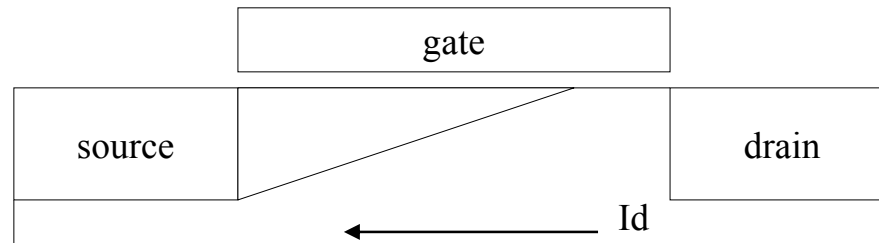
$$V_{gs} > V_t$$

$$V_{ds} < V_{gs} - V_t$$



$$V_{gs} > V_t$$

$$V_{ds} = V_{gs} - V_t$$



$$V_{gs} > V_t$$

$$V_{ds} > V_{gs} - V_t$$

Leakage and sub-threshold current

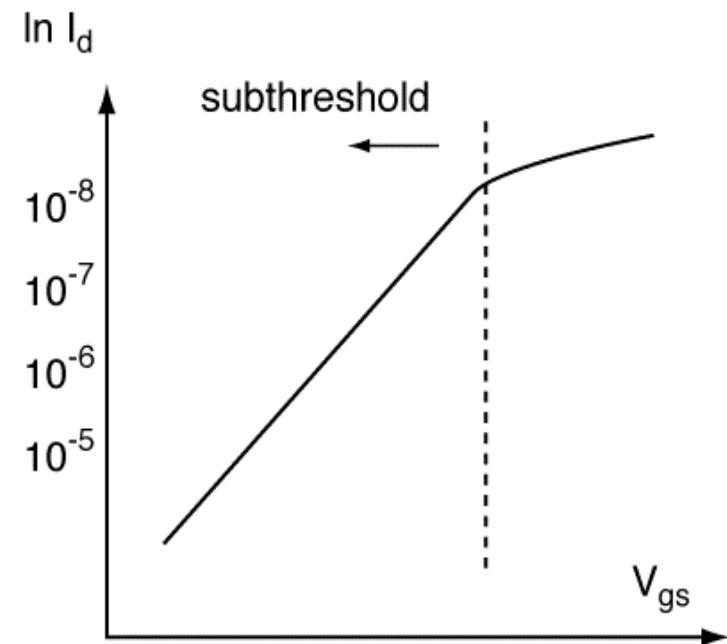
- A variety of leakage currents draw current away from the main logic path.
- Leakage currents cause static power dissipation.
- The sub-threshold current is one particularly important type of leakage current.

Types of leakage current

- Weak inversion current (sub-threshold current).
- Reverse-biased pn junctions.
 - ❖ Follows diode law: $I_1 = I_{lo}(e^{qV_d/kT} - 1)$
 - ❖ I_{lo} typically a few tenths of nanoamp.
- Drain-induced barrier lowering.
- Gate-induced drain leakage.
- Punch-through currents.
- Gate oxide tunneling.
- Hot carriers.

Sub-threshold current

- Sub-threshold current: $I_{\text{sub}} = k e^{[(V_{\text{gs}} - V_t)/(S/\ln 10)]} [1 - e^{-qV_{\text{ds}}/kT}]$
- Sub-threshold slope S characterizes weak inversion current.
- Subthreshold current is an exponential function of gate voltage
- Sub-threshold current is a function of V_t .
 - ❖ Can adjust V_t by changing the substrate bias to control leakage.



The modern MOSFET

Features of deep submicron MOSFETs:

- ❖ epitaxial layer for heavily-doped channel;
- ❖ reduced area source/drain contacts for lower capacitance;
- ❖ lightly-doped drains to reduce hot electron effects;
- ❖ silicided poly, diffusion to reduce resistance.

Circuit simulation

- Circuit simulators like Spice numerically solve device models and Kirchhoff's laws to determine time-domain circuit behavior.
- Numerical solution allows more sophisticated models, non-functional (table-driven) models, etc.

Spice MOSFET models

- Level 1: basic transistor equations of Section 2.2; not very accurate.
- Level 2: more accurate model (effective channel length, etc.).
- Level 3: empirical model.
- Level 4 (BSIM): efficient empirical model.
- New models: level 28 (BSIM2), level 47 (BSIM3).

Some Spice model parameters

- L , W : transistor length width.
- K_P : transconductance.
- GAMMA : body bias factor.
- A_S , A_D : source/drain areas.
- C_{JSW} : zero-bias sidewall capacitance.
- C_{GBO} : zero-bias gate/bulk overlap capacitance.